

2 4-27-00
PB.
EL 373342021

1 Inventor: Werner Juengling

2 Title: Semiconductor Processing Methods of Forming Devices on a
3 Substrate, Forming Device Arrays on a Substrate, Forming
4 Conductive Lines on a Substrate, and Forming Capacitor Arrays
5 on a Substrate, and Integrated Circuitry

6 Assignee: Micron Technology, Inc.



7 INFORMATION DISCLOSURE STATEMENT

8 PURSUANT TO 37 C.F.R. §§1.56, 1.97 AND 1.98

9 In compliance with 37 C.F.R. §§1.56, 1.97 and 1.98, your attention is
10 directed to the United States patents and other references listed on the
11 attached Form PTO-1449.

12 The listed references were cited by, or submitted to, the Office in the
13 parent, co-pending application of the above-identified application. The above-
14 identified application is a divisional of co-pending application Serial No.
15 09/036,701 filed March 6, 1998. Such prior disclosure is sufficient for the
16 above-identified application as far as copies of the references are concerned.
17 37 C.F.R. §1.98(d) and MPEP §609(2). No admission is made regarding
18 whether all the submitted references are prior art.

19 Citation of these references is respectfully requested.

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21 Dated: 10/21/99

Attorney:

Respectfully submitted,

David G. Latwesen, Ph.D.

Reg. No. 38,533

WELLS, ST. JOHN, ROBERTS,
& GREGORY & MATKIN P.S.